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storing the signal corresponding to the pixel signal on the capacitive storage node.

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resetting the pixel;
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10. The method of claim 9 including:

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(The following information was obtained from the records of the Federal Bureau of Investigation, Department of Justice.)

13. The method of claim 12 including:

resetting the pixel after storing the signal corresponding to the pixel signal in the processing circuit;

subsequently reading out a reset signal through the n-MOS source-follower;

passing the reset signal through the p-MOS source-follower to the processing circuit; and

storing a signal corresponding to the reset signal in the processing circuit.

14. The method of claim 13 wherein, prior to passing the reset signal through the p-MOS source-follower, a second capacitive storage node in the processing circuit is clamped to a voltage level higher than the reset signal appearing at the input to the p-MOS source-follower.

15. The method of claim 13 including converting a difference between the pixel and reset signals stored by the processing circuit to a corresponding set of digital signals.

16. An imager comprising:

a pixel readout line;

an active pixel sensor including an n-MOS source-follower through which signals sensed by the sensor can be read out to the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

a signal processing circuit that can be coupled to the pixel readout line; and

a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level less than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out through the n-MOS source-follower to the pixel readout line and to be stored by the processing circuit.

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a pixel readout line

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$\Gamma_{\text{eff}}^{(n)}(\vec{k})$ from eq. (6) can be written as

the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

a signal processing circuit;

a p-MOS source-follower having an output that can be coupled
5 to the processing circuit; and

a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level less than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out
10 through the n-MOS source-follower to the pixel readout line and to be passed to the processing circuit through the p-MOS source-follower.

23. The imager of claim 22 wherein the controller is
15 configured to provide a control signal to cause a capacitive storage node in the processing circuit to be clamped to a voltage greater than the sensor signal at an input to the p-MOS source-follower, wherein the storage node is clamped before passing the sensor signal through the p-MOS source-
20 follower to the processing circuit, and wherein the controller is configured to provide a control signal to cause an output of the p-MOS source-follower subsequently to be coupled to the storage node in the processing circuit.

24. The imager of claim 23 wherein the processing circuit
25 includes a switch that is coupled to the storage node and that selectively can be closed to clamp the storage node to the voltage greater than the sensor signal, and wherein the controller is configured to provide a control signal to cause
30 the switch in the processing circuit to be temporarily closed before causing the output of the p-MOS source-follower to be coupled to the storage node.

25. The imager of claim 23 wherein, when the output of the
35 p-MOS source-follower is coupled to the storage node, the

processing circuit stores a signal corresponding to the sensor signal, and wherein the controller is configured to provide control signals to cause the reset switch subsequently to be enabled, and to cause a reset signal to be read out from the sensor through the n-MOS source-follower and passed through the p-MOS source-follower to the processing circuit such that the processing circuit stores a signal corresponding to the reset signal on a second capacitive storage node.

10 26. A method of processing pixel levels, the method comprising:

clamping a pixel readout line to a voltage level greater than a voltage corresponding to a pixel signal;

subsequently coupling the pixel readout line to an output of a p-MOS source-follower and reading out the pixel signal onto the pixel readout line through the p-MOS source-follower; and storing a signal corresponding to the pixel signal that was read out.

20 27. The method of claim 26 wherein clamping the pixel readout line is performed while processing a previously-stored pixel signal.

28. The method of claim 26 including:

25 clamping a capacitive storage node in a pixel signal processing circuit to a voltage greater than a voltage corresponding to the pixel signal appearing on the pixel readout line;

subsequently coupling the pixel readout line to the storage node in the processing circuit; and

storing the signal corresponding to the pixel signal on the capacitive storage node.

29. The method of claim 28 wherein the storage node is clamped to substantially the same voltage and at about the

[illegible]

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subsequently reading out a reset signal through the p-MOS

source-follower;

passing the reset signal through the n-MOS source-follower to the processing circuit; and

storing a signal corresponding to the reset signal in the
5 processing circuit.

34. An imager comprising:

a pixel readout line;

an active pixel sensor including a p-MOS source-follower
10 through which signals sensed by the sensor can be read out to the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

a signal processing circuit that can be coupled to the pixel readout line; and

15 a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level greater than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out through the p-MOS source-follower to the pixel readout
20 line and to be stored by the processing circuit.

35. The imager of claim 34 wherein the processing circuit includes a capacitive storage node, and wherein the controller is configured to provide control signals to cause the
25 capacitive storage node to be clamped to a voltage greater than a voltage corresponding to the sensor signal appearing on the pixel readout line, and subsequently to cause the pixel readout line to be coupled to the storage node.

30 36. The imager of claim 35 wherein the processing circuit includes a second capacitive storage node, and wherein the controller is configured to provide control signals to cause the reset switch in the pixel to be enabled, and subsequently to cause a reset signal to be read out onto the pixel readout
35 line through the p-MOS source-follower, and to cause a signal

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that corresponds to the reset signal to be stored on the second capacitive storage node.

37. An imager comprising:

5 a pixel readout line;

an active pixel sensor including a p-MOS source-follower through which signals sensed by the sensor can be read out to the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

10 a signal processing circuit;

an n-MOS source-follower having an output that can be coupled to the processing circuit; and

a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level

15 greater than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out through the p-MOS source-follower to the pixel readout line and to be passed to the processing circuit through the n-MOS source-follower.

20 38. The imager of claim 37 wherein the controller is configured to provide a control signal to cause a capacitive storage node in the processing circuit to be clamped to a voltage less than the sensor signal at an input to the n-MOS source-follower, wherein the storage node is clamped before
25 passing the sensor signal through the n-MOS source-follower to the processing circuit, and wherein the controller is configured to provide a control signal to cause an output of the n-MOS source-follower subsequently to be coupled to the
30 storage node in the processing circuit.

39. The imager of claim 37 wherein the processing circuit includes a switch that is coupled to the storage node and that selectively can be closed to clamp the node to the voltage
35 less than the sensor signal, and wherein the controller is

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The following is a list of the names of the persons who have been appointed to the various positions in the Department of the Interior, for the term of years indicated: